Maximizing Energy Efficiency in Your Designs

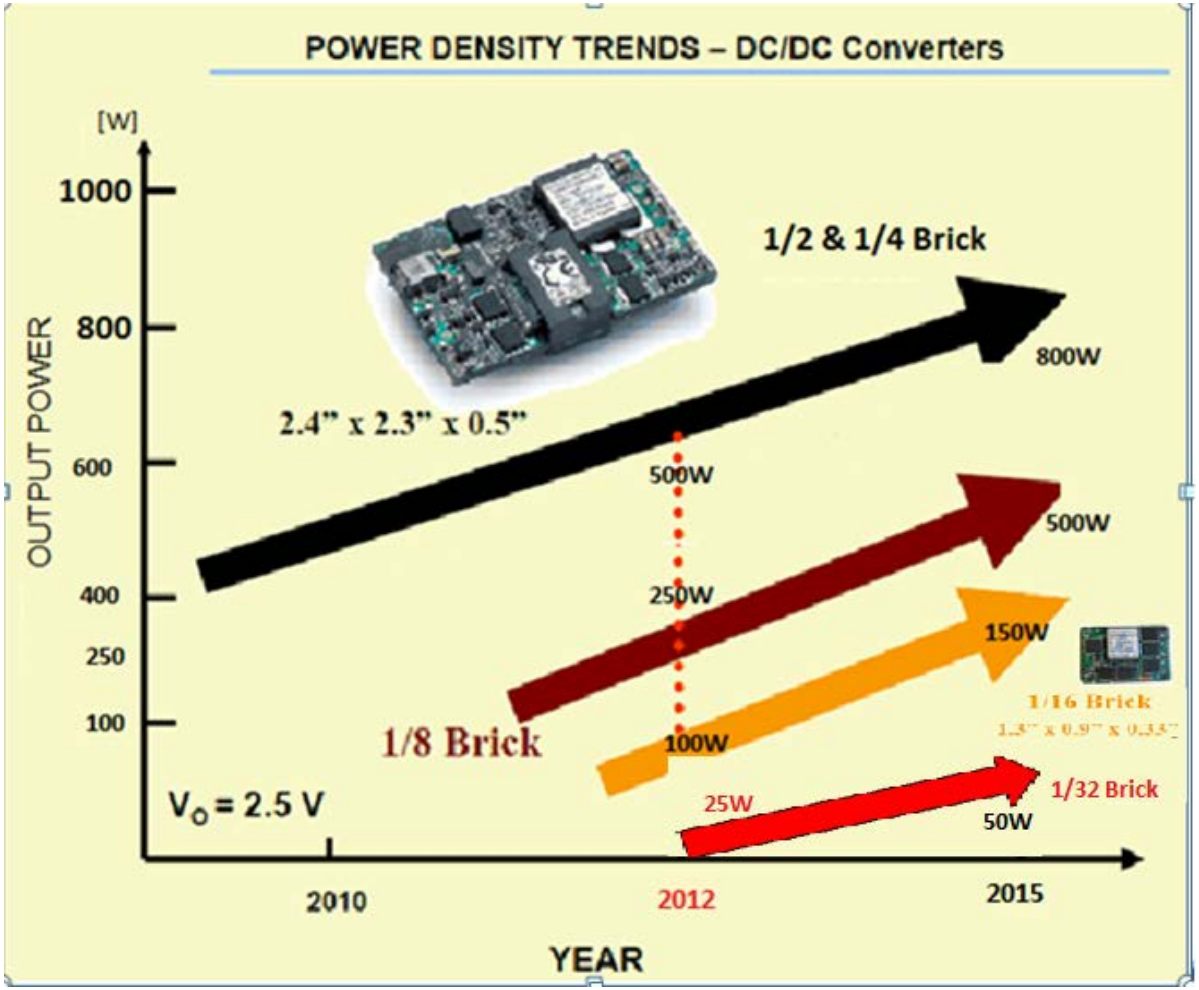
Fairchild's Advanced MOSFETs with Innovative Packaging and Technologies

Mike Speed – Marketing Director (CCI MOSFET Segment)

Solutions for Your Success™

Power Density Progression

Fairchild enables high power density with differentiated MOSFET Technology



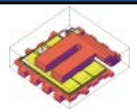
FAIRCHILD SEMICONDUCTOR®

Agenda

- Latest in MOSFET Technology
  - Packaging innovation
  - Silicon technology advancement
  - Silicon differentiation in mid-voltage
- Case Studies
  - Case study in isolated DC-DC
    - Dual 5x6 symmetrical for bridge applications
  - Case study in non-isolated point-of-load
    - Dual power clip asymmetrical dual 25V
- Power-over-Ethernet applications – MOSFET selection
  - Power source equipment (PSE)
  - Power device (PD)

Packaging Innovation: Smaller, Simpler, Thinner

Power Clip: Singles and Dual MOSFETs



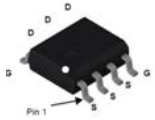
Power Clip 33 Single

Power Clip 56 Single

Power Clip 33 and 56 Duals

- Industry's best die to footprint ratio QFN package enables higher power density
- Cu Clip interconnect and Flip Chip LS reduces package resistance & inductance for reduced power loss and low thermal impedance
- Power clip dual design enables optimized board layout for POL converter and multiphase designs

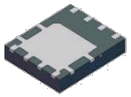
Leaded



SO8 30/20

Leadless PQFN

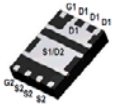
Better Thermals



5x6 and 3x3 Singles 25/12

Dual MOSFETs

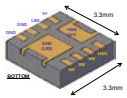
Half the Area



5x6 Dual MOSFET: Power Stage

Power Clip Duals

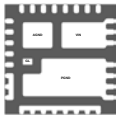
Highest Performance Dual MOSFET



3x3 and 5x6Dual MOSFET: Power Clip

SPS / TinyBuck® Regulators

Fully Integrated Analog Solution



5x5 Integrated Solution

2008 2012 2013

Performance and Power Density

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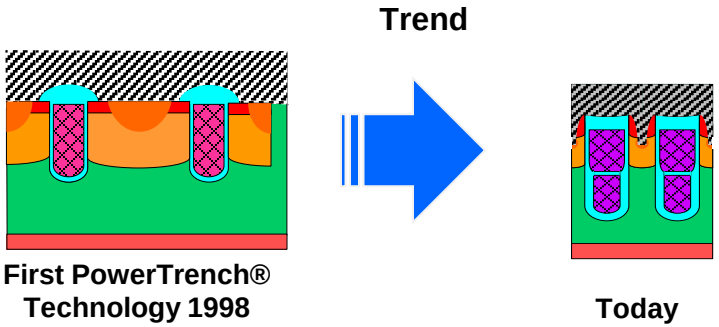
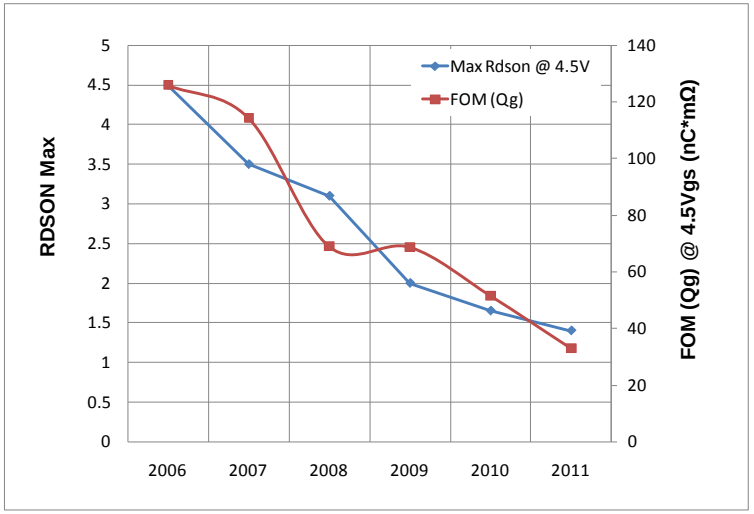
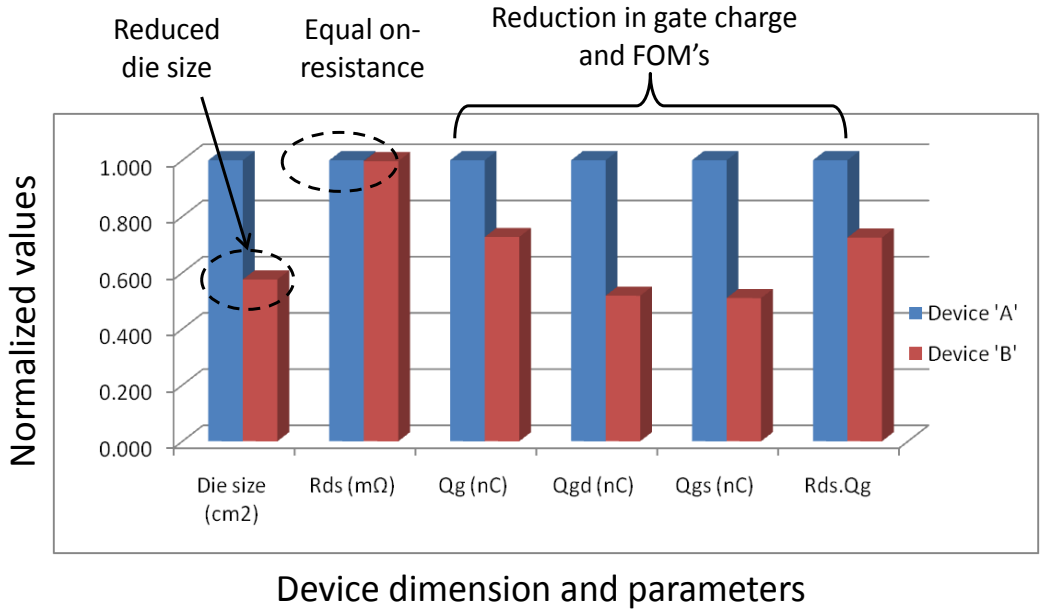
Technology Progression - N Channel 25 V to 150 V



- Continuous FOM improvement
- Increasing power density
- Small form factor
- Improving efficiency





Device dimension and parameters

Improvements in trench technology lead to better $R_{DS(ON)}$, Q_G, C_{OSS} and FOM

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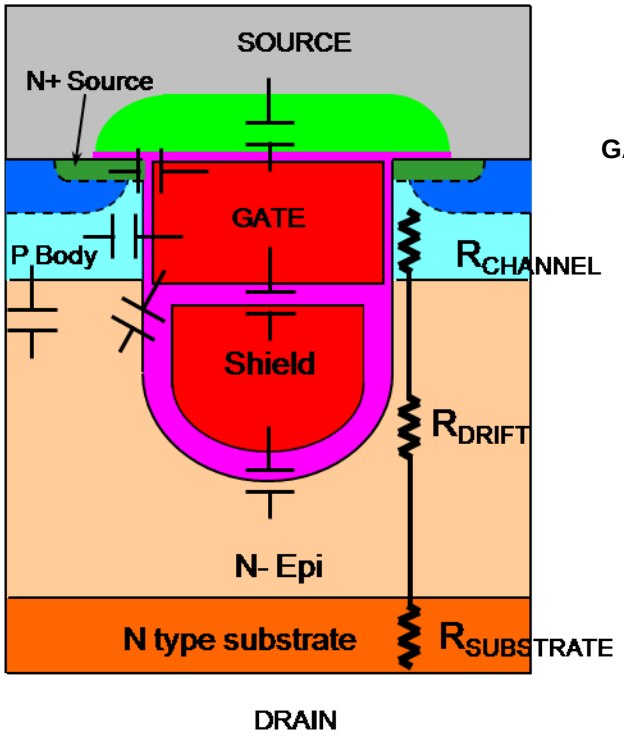
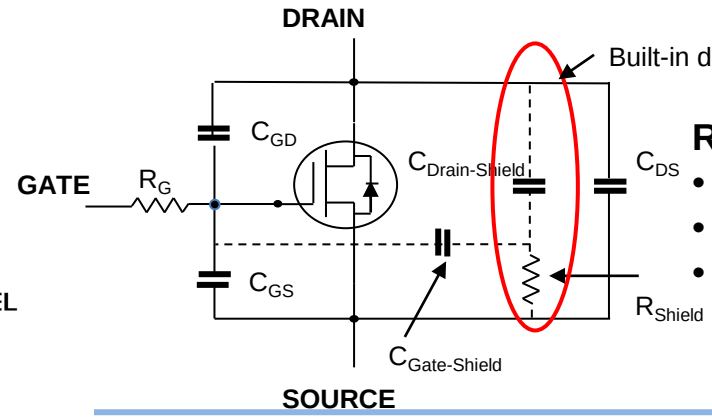
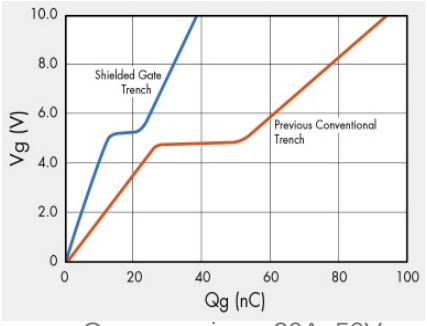
Benefits of Shielded Gate Technology





Reduced switch node ringing
- Result from Rshield and Cshield
- EMI reduction
- No external snubbers required

Reduced gate charge
- Superior switching performance
- Improved Q_{GS} /Q_{GS} ratio increasing immunity to cross conduction



Q_G comparison: 20A, 50V

Shielded Gate brings additional advantages to conventional trench technologies

Rds(on) Vg = 10V, 200A/cm²	
Vds = 30V	Vds = 100V
R_{Chan} = 47%	R_{Chan} = 16%
R_{EPI} = 29%	R_{EPI} = 78%
R_{Sub} = 24%	R_{Sub} = 6%

Reduced $R_{DS(ON)}$
- Increased drift region doping reduces on resistance at the epi layer

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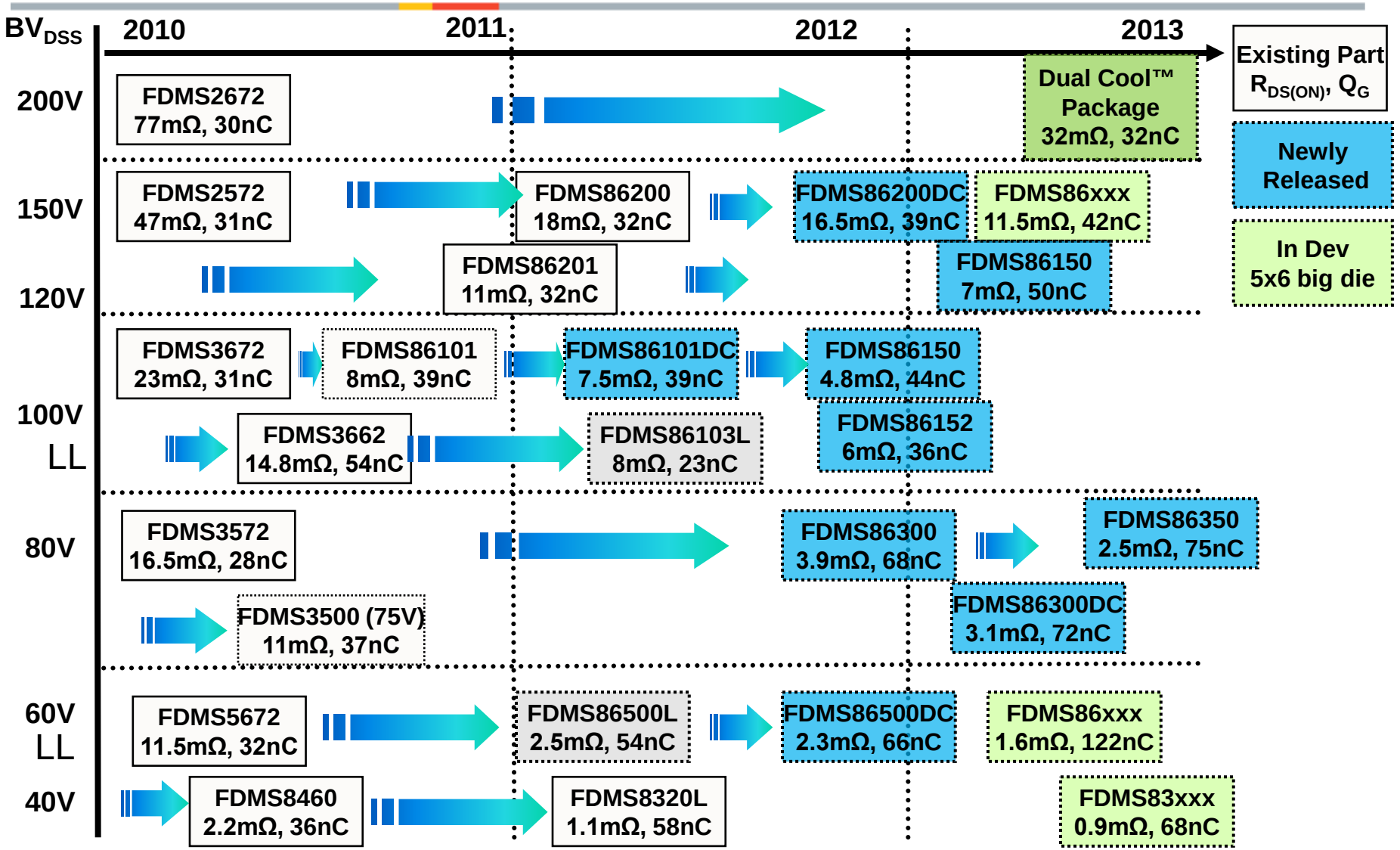
UltraFET Trench vs. Shielded Gate Technology (150 V)

	UltraFET Trench			Shielded Gate		
Package	**Part number**	**$R_{DS(on)}$ @ V_{GS} = 10 V**	**Q_G nC**	**Part number**	**$R_{DS(on)}$ @ V_{GS} = 10 V**	**Q_G nC**
Power 56	FDMS2572	47 mΩ	31	FDMS86252	50 mΩ	**11**
SO8	FDS2582	66 mΩ	19	FDS86242	67 mΩ	**8.9**
Power33	FDMC2523P	1.5 Ω	6.2	FDMC86261P	**170 mΩ**	15

Better cost and performance advantages with Shielded Gate Technology

Power 56: Mid-Voltage N Channel Product Roadmap



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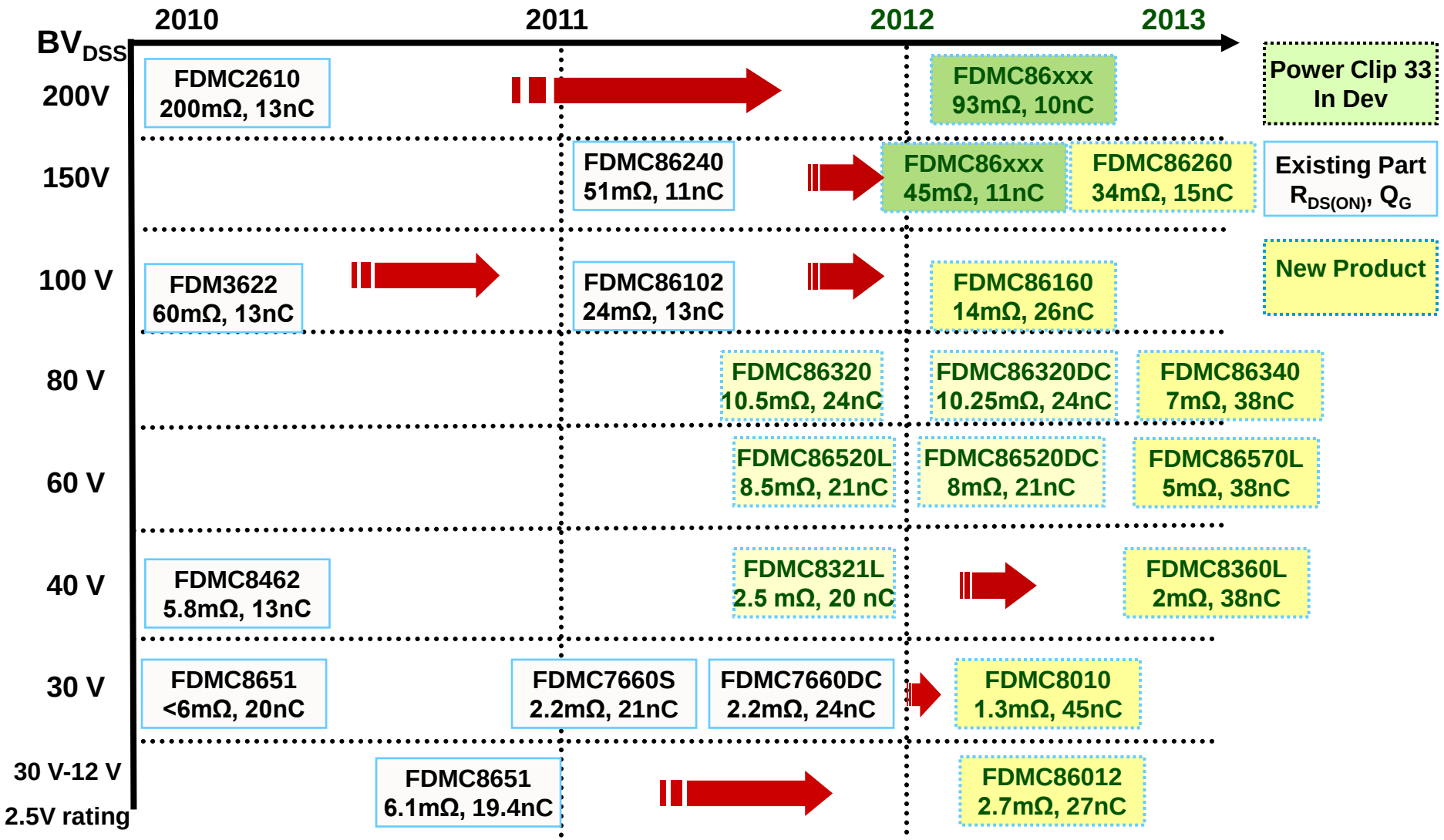
Power 33: 20 to 200 V N Channel Product Roadmap



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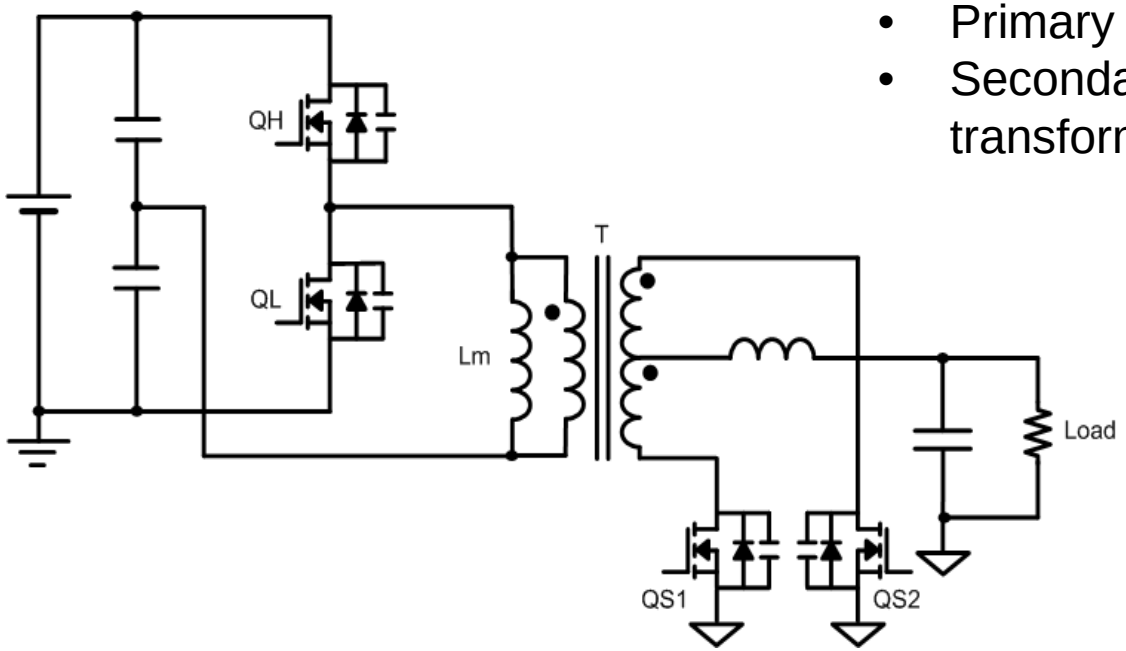
Simplified Power Stage Schematic



- Primary : Half bridge
- Secondary: Center tap secondary transformer & Synchronous rectification

QH & QL Part #	Internal Structure	$R_{DS(ON)}$ (mΩ)	Q_G (nC) V_{GS} = 10 V
FDMS8090	Symmetrical Dual	13	15
FDMS8610	Single	8	55

Primary switch	QH	**FDMS8090 vs. FDMS86101**
	QL	
Secondary switch	QS1	FDMS8023S X 2ea
	QS2	FDMS8023S X 2ea
Transformer	T	Primary : Secondary = 8T : 2T Center tap secondary Lm = 120 uH, Lk = 0.25 uH
Inductor	L	1.2 uH

Evaluation board Overview

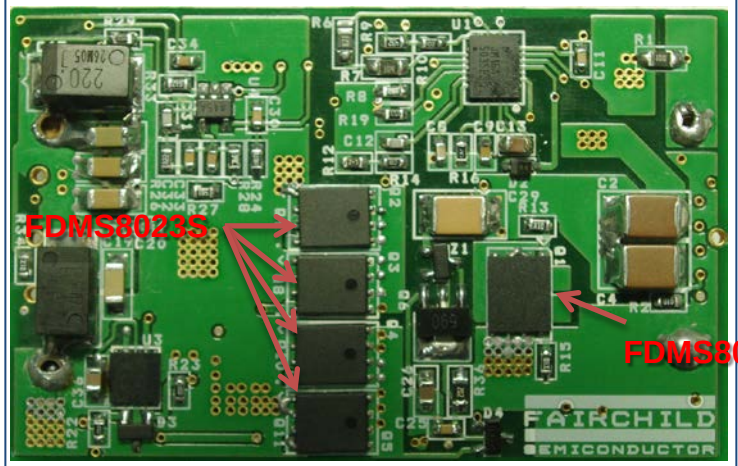
Circuit Conditions

Conditions	Descriptions
Evaluation Board	100W Half-bridge DC-DC
DC-DC Topology	Half bridge
Primary Switch	FDMS8090 or FDMS86101
Secondary Switch	FDMS8023S
PWM controller + Gate driver	LM5035B
V_{IN}	36 ~ 75 V
Primary Vgs	10 V
V_{OUT}	3.3 V
Switching frequency	200 kHz
Maximum load current	30 A
Transformer	DA2025-AL 8T:2T, Lm = 120 uH, Lk = 0.25 uH
Inductor	SER2010-122 1.2 uH
PCB	FR-4 / 8layer Outer copper thickness: 2oz Inner copper thickness: 2oz Total thickness: 2 mm
Running Condition	1 A, 5 A, 10 A, 15 A …30 A 5min. soaking/each step

EVB Vehicle:

Size = 57.9 X 36.9mm; Quarter brick size

Bottom side



Top side

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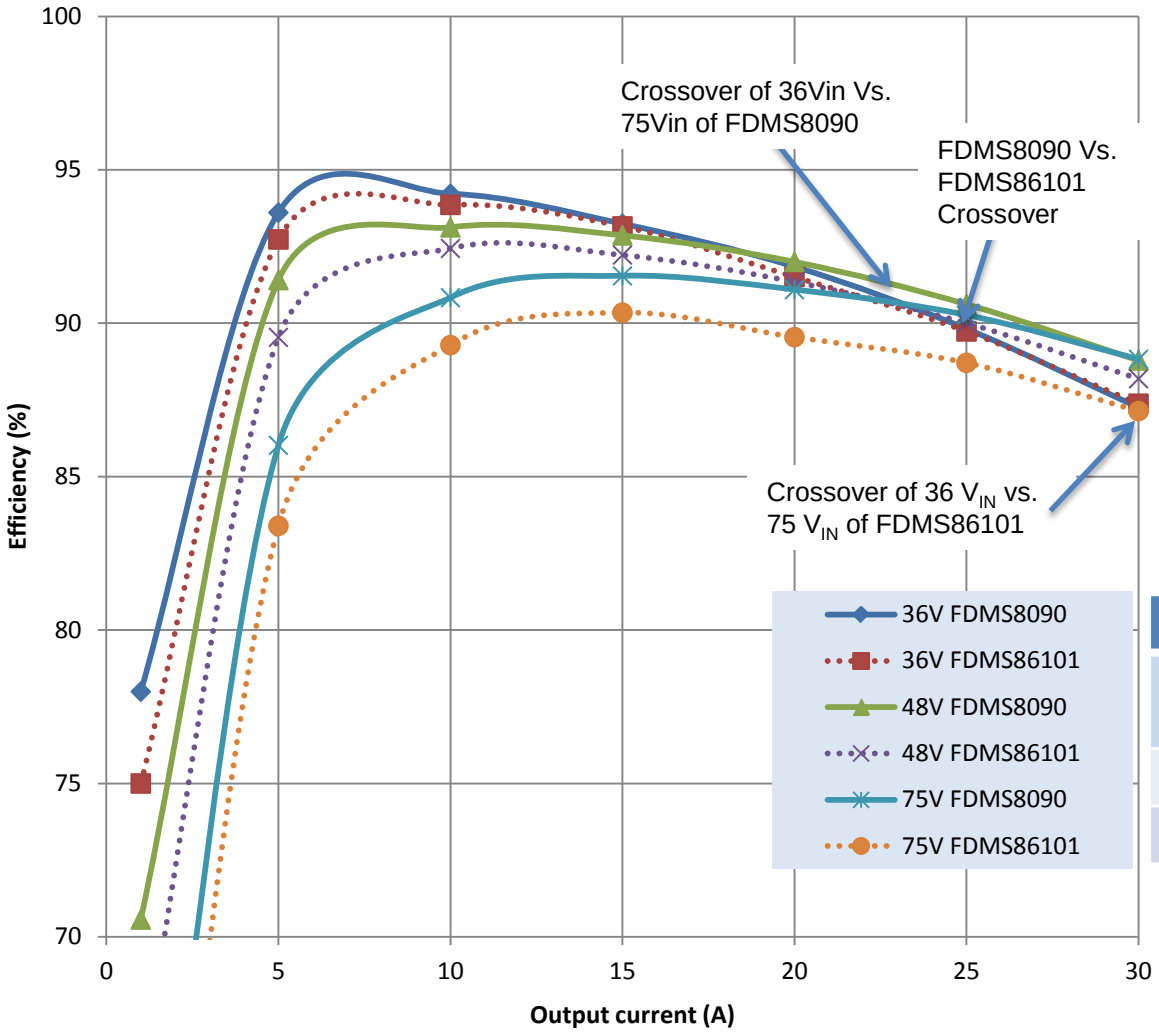
Total Efficiency Comparison

V_{IN} = 36 ~ 75 V, V_{OUT} = 3.3 V / I_{OUT} = 1 ~ 30 A



- FDMS8090 vs. FDMS86101
  - Efficiency crossover is @ 25 A output current and 36 V input voltage
- FDMS8090
  - Higher efficiency in all other input voltage and output current ranges
  - More well-balanced Q_G and $R_{DS(ON)}$
- FDMS86101
  - Crossover of 36 VIN vs. 75V_{IN} is at 30 A output current
  - Switching loss is the main factor in the evaluation board

	@48 V Input Voltage	
	Maximum Efficiency	Efficiency @ Max. load
FDMS8090	**93.12%**	**88.78%**
FDMS86101	**92.43%**	**88.18%**

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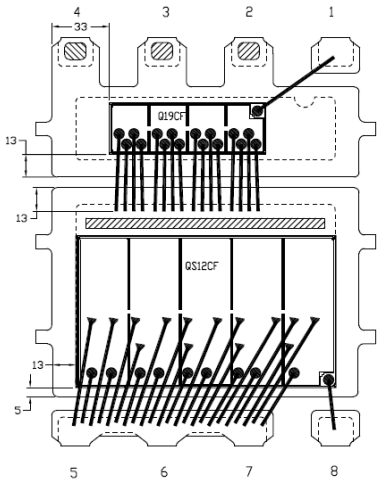
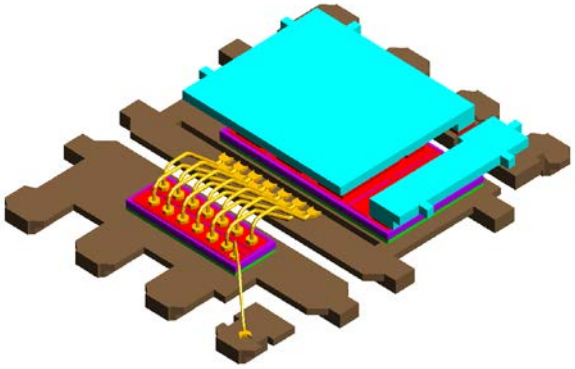
Package Evolution – Power Stage MOSFETs

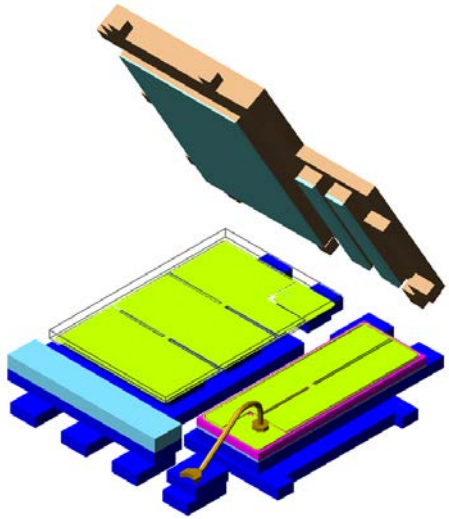


Conventional Technology 2007-2009



Clip Technology 2010

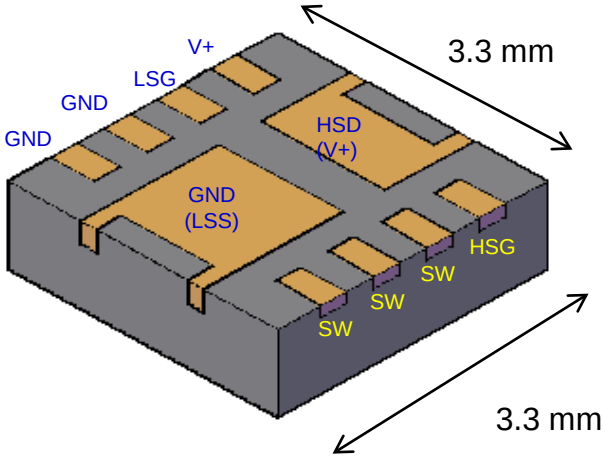
- Reduction in internal parasitic
- Optimized thermal performance due to clip
- Reduction in $R_{DS(ON)}$ on low side
- Allows lower package resistance

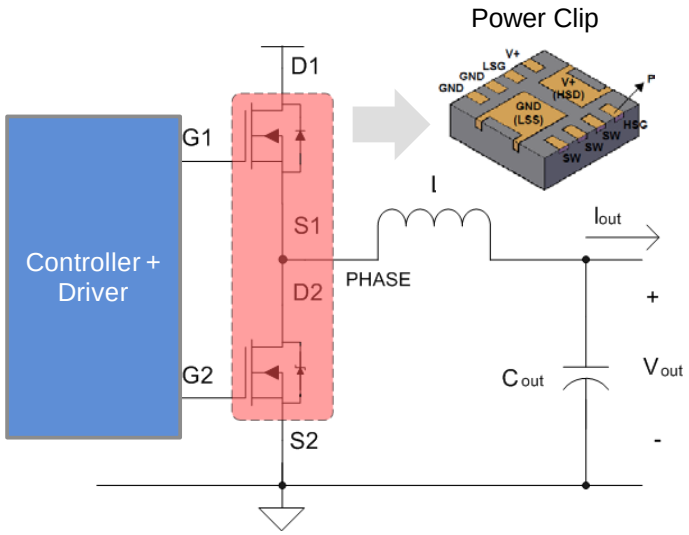


Power Clip Technology 2012

- Increase of power density to footprint ratio
- Further parasitic reduction and $R_{DS(ON)}$ improvement
- Ease of board layout

Dual Power Clip MOSFET





Features

- Control + Synchronous MOSFETs in a single 3x3 package
- 3x3: extremely low R_{DSON} (5.8mΩ HS, 1.8mΩ LS)
  - Flip chip LS
- Wireless power path interconnections eliminate unwanted parasitic inductance and resistance
- Low output capacitance, low figure of merit , improved HS transconductance

Benefits

- Highest current capability 3x3 dual in the industry (15A – 25A)
- Replaces multiple 3x3 or 5x6 components
- Low junction and board temperature: Optimized thermal pad placement enhances power dissipation.
- Highest efficiency at light and heavy loads – Shielded gate

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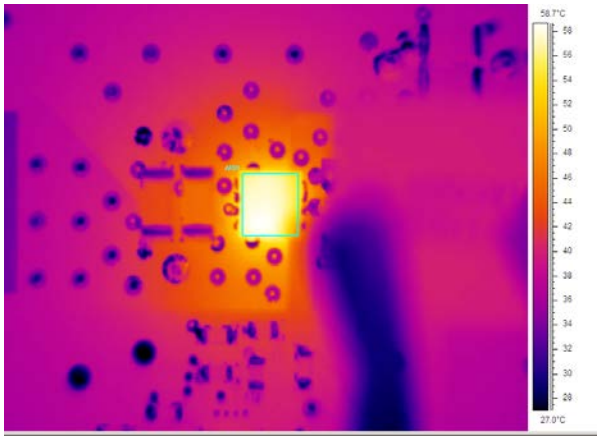
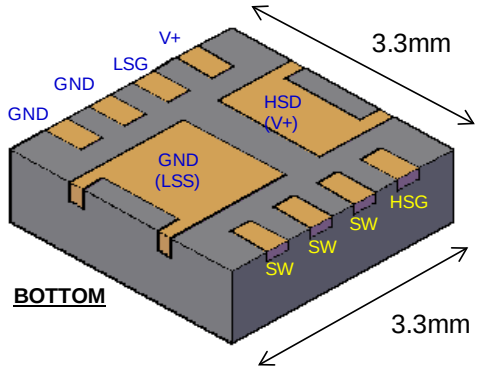
Optimal Thermal Performance

Thermal Capture for the Device in Buck Converter Configuration



FDPC8011S
56.8'C @ 20A

Test Conditions:
V_{IN}=12 V, V_{OUT}=1 V, F_{SW} =600 kHz
5 V Gate Drive



Power Clip 3.3x3.3 mm^2 Package

Dual Power Clip footprint provides optimized thermal performance

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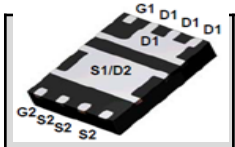
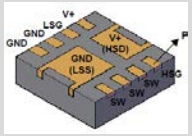
Power Stage & Power Clip Dual MOSFET Portfolio

Power Stage 5x6 Duals

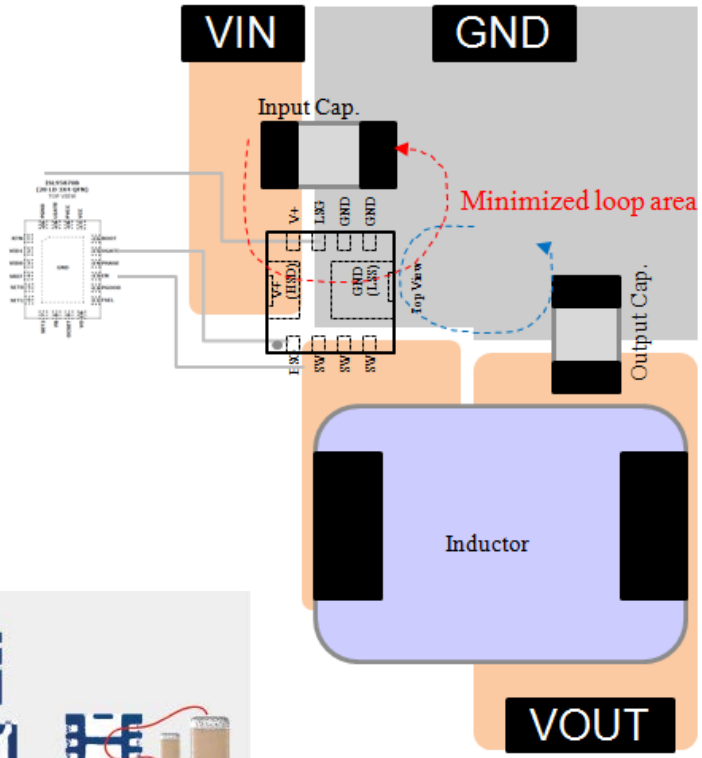
	Size	Imax	BV_{DSS}	VGS_{MAX}	$R_{DS(ON)}$ Max (mΩ) 4.5V V_{GS}		Q_G Typ (nC) @ V_{GS} = 4.5 V_{GS}		C_{oss} Typ (pF)	Status
					High Side	Low Side	High Side	Low Side	Low Side	
FDMS3620S	5x6	>30A	25V	12v	5.5	1.2	12	50	1828	Released
FDMS3622S		25-30A			5.7	1.6	12	40	1405	Released
FDMS3624S		20-25A			5.7	2.2	12	27	946	Released
FDMS3626S		15-20A			5.7	3.2	12	19	716	Released
FDMC8200S	3x3	<6A	30V	20v	20	32	3.1	7.2	495	Released

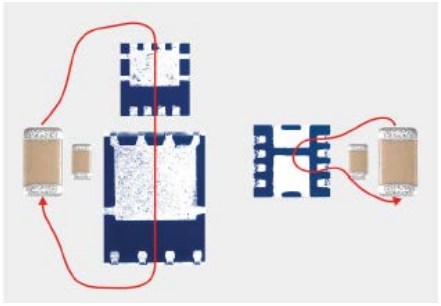
Power Clip Duals

	Size	Imax	BV_{DSS}	VGS_{MAX}	$R_{DS(ON)}$ Max (mΩ) 4.5 V V_{GS}		Q_G Typ (nC) @ V_{GS} = 4.5 V_{GS}		C_{oss} Typ (pF)	Status
					High Side	Low Side	High Side	Low Side	Low Side	
FDPC8011S	3.3x 3.3	15-20A	25V	12V	7.3	2.1	9	30	1126	Released
FDPC8013S		10-15A	30V	20V	9.6	2.7	6	21	997	Released
FDPC80xxx	**5x6**	20-30A	25V	12V	4.5	1.6	13	36	1256	Sampling
FDPC80xxx		>30A	25V	12V	4.5	1.2	13	49	1698	Sampling

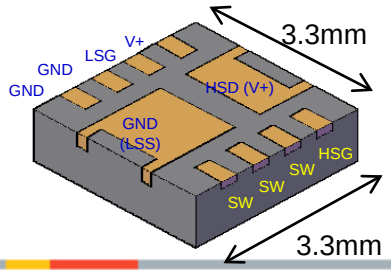
Layout Benefits - Power Clip Dual

Point of Load Dual



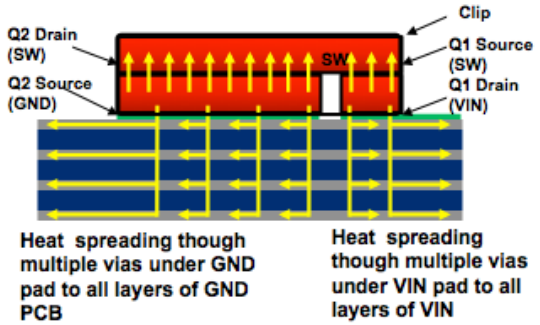


Switching current path



Point of Load layout

- Heat easily dissipates through the GND and VIN planes, which are better suited for this function



- Power train loop is tighter which further reduces conduction loss

- HF switching loop much smaller reduces parasitic for high frequency operation

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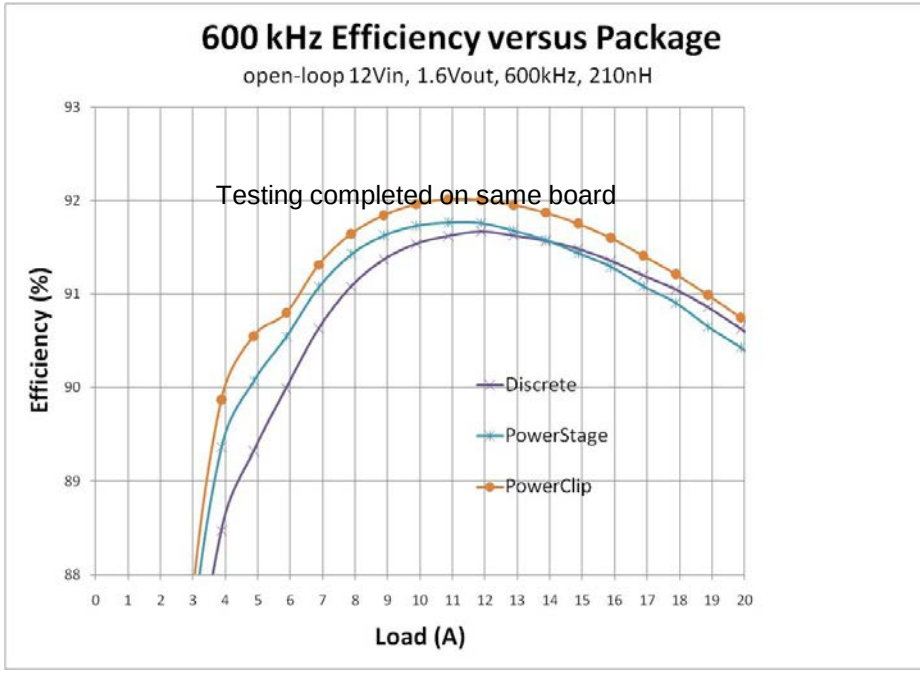
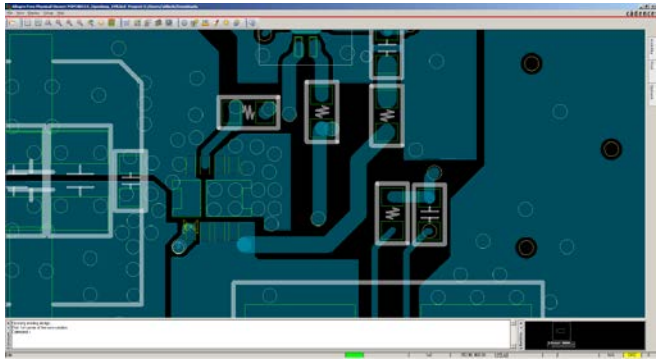
Power Clip Dual 3x3 Efficiency Data – FDPC8011S



Package	Device		4.5 v Rdson Max	Q_G Typ @ V_{GS} = 4.5 V_{GS} (nC)
Discrete	FDMC8588	HS	5.7	12
	FDMS8560S	LS	2.1	32
Power Stage	FDMS3624S	HS	5.7	12
		LS	2.2	27
Power Clip	FDPC8011S	HS	7.3	9
		LS	2.1	30



- Test Conditions
  - V_{IN} = 12 V
  - V_{OUT} = 1.6 V
  - F_{SW} = 600kHz
- 25ºC environment
- No forced air
- PCB has 6 layers
  - All 1 oz copper
  - HS G trace top layer
  - LS trace on top and in three layers

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Lower HS and LS Source Inductance Minimizes Switching Noise

Large Footprint 3x3 & 5x6, Medium footprint 1x5x6, Small footprint 1x3.3x3.3

Discrete vs. Power Clip at HS Turn-On

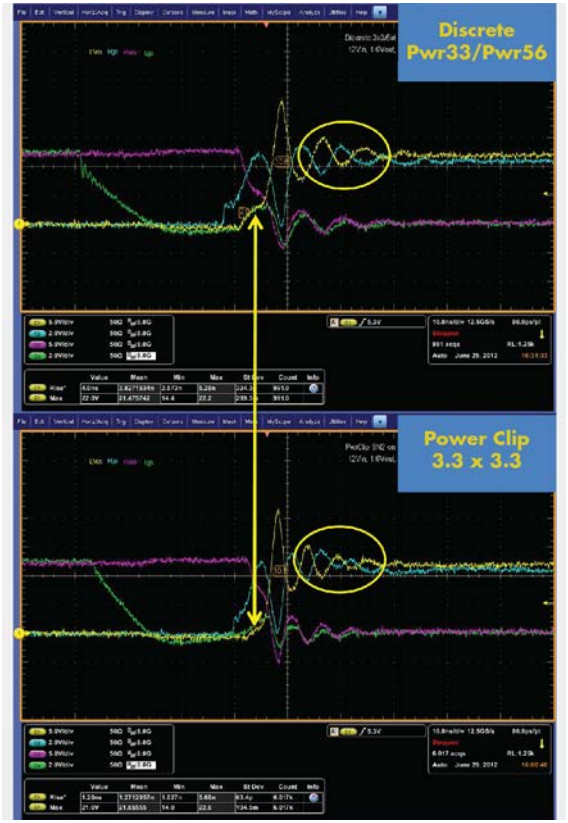


Figure 1

	Large Footprint	Medium Footprint	Small Footprint	Inductance
HS Drain	0.156	0.146	0.049	nH
HS Source	0.386	0.498	0.127	nH
LS Drain	0.205	0.191	0.073	nH
LS Source	0.593	0.349	0.026	nH

- Power Clip has a reduced PCB layout and lower parasitic inductance.
- Lower layout inductance seen in Vsw higher ring freq (fig 1) and in reduced HS peak V_{DS} ring (fig 2).
- Lower LS S inductance seen in smaller initial Vsw rise (fig 1) and in reduced Vsw undershoot at HS turn on (fig 2).

Discrete vs. Power Clip at HS Turn-Off

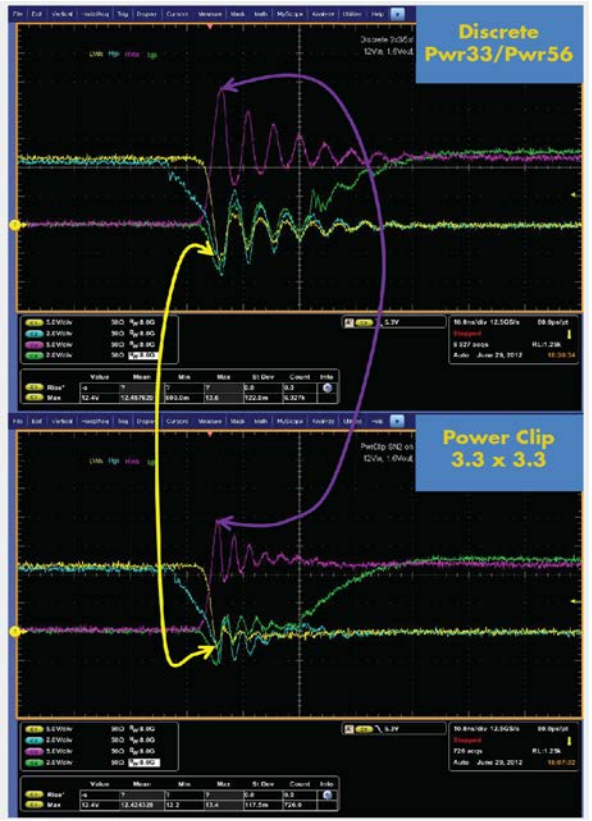


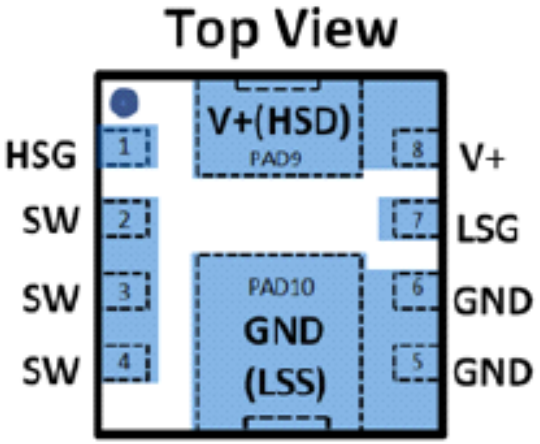
Figure 2

FAIRCHILD SEMICONDUCTOR®

Recommended PCB Layout Guidelines

Power Clip Asymmetrical Dual MOSFET

- Power Clip is a high power density solution and all high current flow paths, such as V+(HSD), SW and GND(LSS) should be short and wide for minimal resistance and inductance.
- V+(HSD) and GND(LSS) are the primary heat flow paths for the Power Clip.



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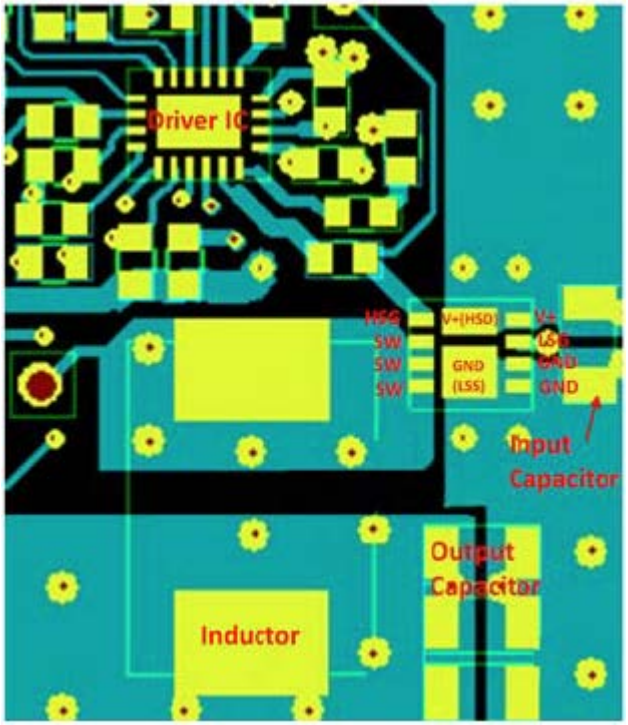
Recommended PCB Layout Guidelines

Power Clip Asymmetrical Dual MOSFET

- The Driver IC should be placed relatively close to **HSG** and **LSG** to minimize gate drive trace inductance. (External Register could be added to adjust switching speed.)
- Use short and wide trace for **SW** because it is not only a high current path but also a high noise region due to switching voltage transients. (External RC snubber could be added to reduce voltage spike which is very rare in *Power Clip* package.)
- Use large copper areas for $\mathbf{V_{IN}}$.
- The input ceramic bypass capacitor between $\mathbf{V_{IN}}$ and $\mathbf{G_{ND}}$ should be placed as close as possible to the MOSFET to help reduce parasitic inductance and high frequency ringing
- Use large copper areas and multiple vias for $\mathbf{G_{ND}}$ to have better thermal conductivity.
  - *Power Clip* package has better heat transfer than traditional dual FET

Top View

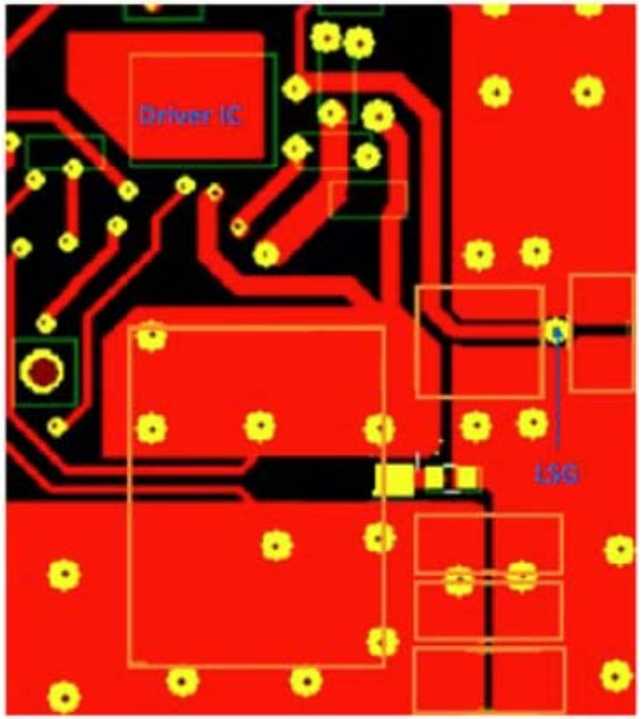


FAIRCHILD SEMICONDUCTOR®

Recommended PCB Layout Guidelines

Power Clip Asymmetrical Dual MOSFET

Bottom View



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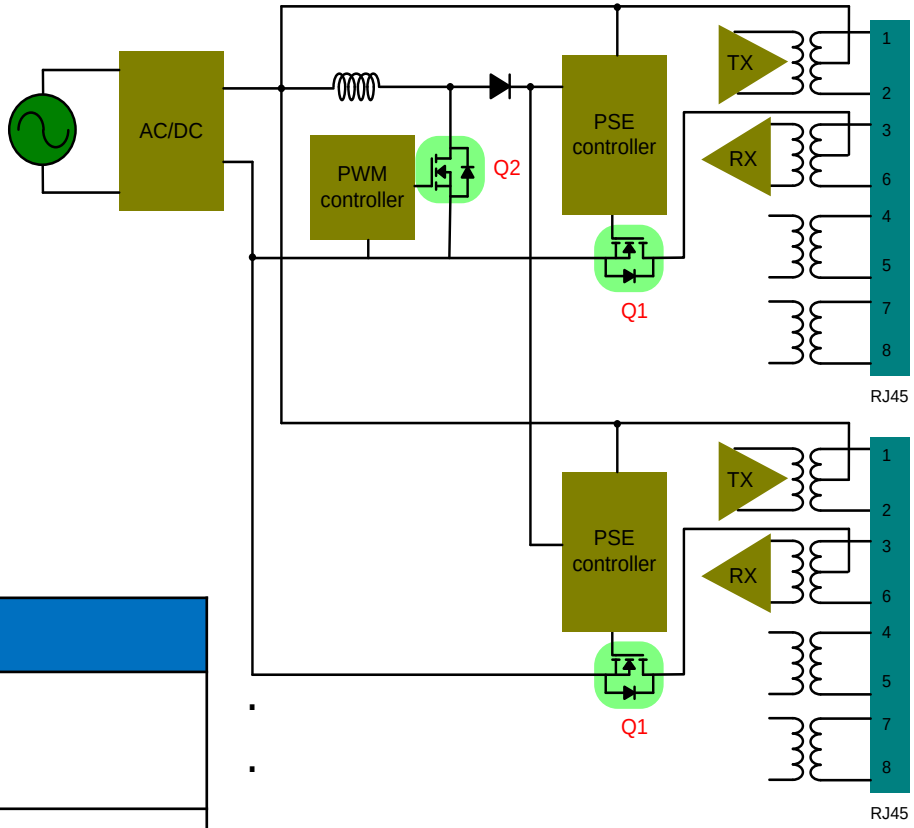
Agenda

- Latest in MOSFET Technology
  - Packaging innovation
  - Silicon technology advancement
  - Silicon differentiation in mid-voltage
- Case Studies
  - Case study in isolated DC-DC
    - Dual 5x6 symmetrical for bridge applications
  - Case study in non-isolated point-of-load
    - Dual power clip asymmetrical dual 25V
- Power-over-Ethernet applications – MOSFET selection
  - Power source equipment (PSE)
  - Power device (PD)

Power over Ethernet – MOSFETs

Power Application Guide for PSE

- The PSE (Power Source Equipment) is the equipment that provides power and data to PDs(Power Devices) via network cables of Ethernet Routers, Switches and Hubs. The PSE's main functions are:
  - Search the link section for a PD
  - Optionally classify the PD
  - Supply power to the link section (only if a PD is detected)
  - Monitor the power on the link section



Requirements		
Q1	Hot swap switching MV MOSFET	• Low $R_{DS(ON)}$ • Wide SOA
Q2	Boost switching MV MOSFET	• High frequency switching • Fast switching

Power over Ethernet - MOSFETs for PSE

Q1 Hot Swap Switching MOSFETs

Package	Part Number	BVdss (V)	V_{GS} (V)	$R_{DS(ON)}$ Max (mΩ) @10Vgs	$R_{DS(ON)}$ Max (mΩ) @6Vgs	I_D (A)	Q_G TYP (nC) @10Vgs	Q_{GD} (nC)	Remark
MLP 3X3	FDMC86102	100	20	24	38	7	13	3.6	Performance
MLP 3X3	FDMC3612	100	20	110	122	3.3	14.4	3.7	Small size
SOT223	FDT3612	100	20	120	130	3.7	14	3.8	Legacy

Q2 Boost Switching MOSFETs

Package	Part Number	BVdss (V)	V_{GS} (V)	$R_{DS(ON)}$ Max (mΩ) @10Vgs	$R_{DS(ON)}$ Max (mΩ) @6Vgs	I_D (A)	Q_G TYP (nC) @10Vgs	Q_{GD} (nC)	Remark
MLP 3X3	FDMC86244	150	20	134	186	2.8	4.2	1	Performance
SSOT6	FDC86244	150	20	144	188	2.3	4.2	1	Small size
SSOT6	FDC2512	150	20	425	475	1.4	8	2.3	Small size

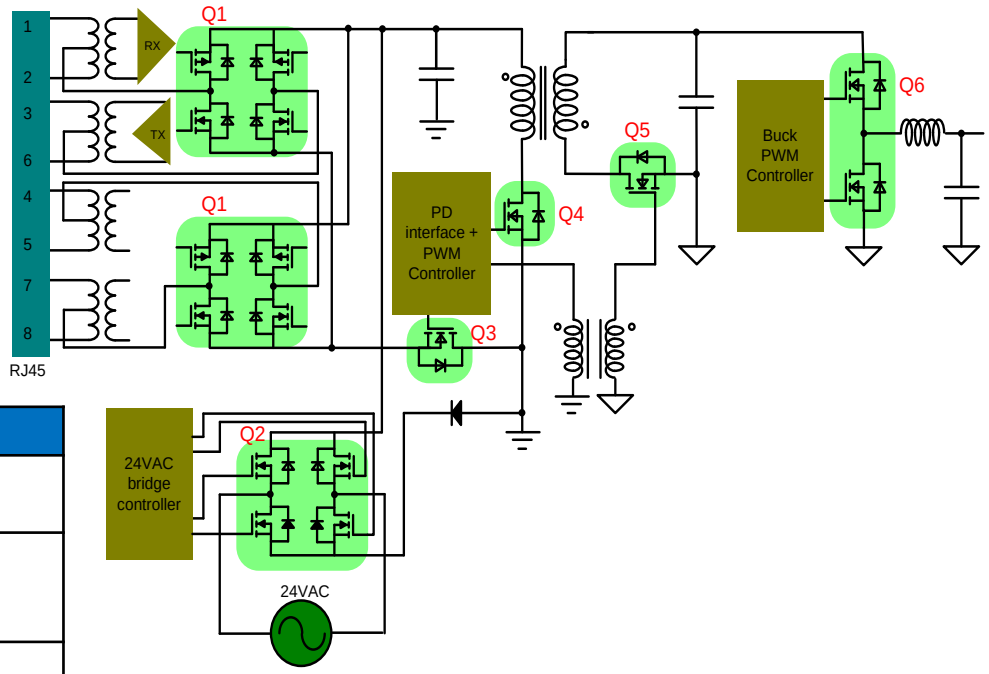
PSE Demo Board

Demo Board	
30W Single-port PSE demo board	User Guide for 30W Single-port PSE demo board

Power over Ethernet – MOSFETs

Power Application Guide for PD

- The Power device (PD) is the device that is either drawing power or requesting power from PSE via network cables of IP telephones, wireless LAN access points, and security IP cameras; without any wall power lines



Requirements		
Q1	Active MOSFET bridge for polarity protection	• Low $R_{DS(ON)}$ • Small package
Q2	Active MOSFET bridge for 24VAC full bridge rectification	• Low $R_{DS(ON)}$ • Small package
Q3	Hot swap switching MV MOSFET	• Low $R_{DS(ON)}$ • Wide SOA
Q4	Flyback Primary switching MV MOSFET	• High frequency switching • Fast switching
Q5	Synchronous rectification MOSFET	• Low $R_{DS(ON)}$ • Fast reverse recovery
Q6	Synchronous Buck switching dual MSOFET	High side MOSFET • Fast switching Low side MOSFET • Low $R_{DS(ON)}$

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Power over Ethernet – MOSFETs for PD

Q1 Active MOSFET Bridge for Polarity Protection

Package	Part Number	BVdss (V)	V_{GS} (V)	$R_{DS(ON)}$ Max (mΩ) @10Vgs	$R_{DS(ON)}$ Max (mΩ) @6Vgs	I_D (A)	Q_G (nC) @10Vgs	Q_{GD} (nC)	Remark
SSOT3	FDN8601	100	20	109	175	2.7	3	0.8	Small Single N
SSOT6	FDC3535	-80	20	183	233	2.1	14	2.7	Small Single N
SSOT6	FDC8602	100	20	350	575	1.2	1.2	0.4	Dual N
SO8	FDS89161	100	20	105	171	2.7	3	0.8	Dual N
SO8	FDS8935	-80	20	183	247	2.1	13	2.6	Dual P
MLP4.5X5	FDMQ8203	100	20	110	175	3	3	0.8	GreenBridge™ Quad N/P
		-80	20	190	235	2.3	14	2.7	
MLP 4.5X5	FDMQ8403	100	20	110	175	3	3	0.8	GreenBridge™ Quad N

Q2 Active MOSFET Bridge for 24VAC Rectification

Package	Part Number	BVdss (V)	V_{GS} (V)	$R_{DS(ON)}$ Max (mΩ) @10Vgs	$R_{DS(ON)}$ Max (mΩ) @6Vgs	I_D (A)	Q_G (nC) @10Vgs	Q_{GD} (nC)	Remark
MLP 4.5X5	FDMQ86530L	60	20	17.5	23	8	23	2.3	GreenBridge™ Quad N
MLP 3X3	FDMC89521L	60	20	17	27	8.2	17	1.9	Dual N
MLP 3X3	FDMC86520L	60	20	7.9	11.7	13.5	45	4.9	Single N
MLP 5X6	FDMS86500L	60	20	2.5	3.7	25	117	11.5	Single N
Dual Cool™ Package MLP 5X6	FDMS86500DC	60	20	2.2	3.3	29	79	20	Performance Single N

Power over Ethernet – MOSFETs for PD

Q3 Hot Swap Switching MOSFETs

Package	Part Number	BVdss (V)	V_{GS} (V)	$R_{DS(ON)}$ Max (mΩ) @10Vgs	$R_{DS(ON)}$ Max (mΩ) @6Vgs	I_D (A)	Q_G TYP (nC) @10Vgs	Q_{GD} (nC)	Remark
MLP 3X3	FDMC86102	100	20	24	38	7	13	3.6	Performance
MLP 3X3	FDMC3612	100	20	110	122	3.3	14.4	3.7	Small size
SOT223	FDT3612	100	20	120	130	3.7	14	3.8	Legacy

Q4 Flyback Primary Switching MOSFETs

Package	Part Number	BVdss (V)	V_{GS} (V)	$R_{DS(ON)}$ Max (mΩ) @10Vgs	$R_{DS(ON)}$ Max (mΩ) @6Vgs	I_D (A)	Q_G (nC) @10Vgs	Q_{GD} (nC)	Remark
SSOT3	FDN86246	150	20	261	359	1.6	2.9	0.8	IEEE802.3af
SSOT6	FDC86244	150	20	146	182	2.2	4	1	IEEE802.3af
SO8	FDS86242	150	20	67	98	4.1	8.9	2	IEEE802.3at
MLP 3X3	FDMC86244	150	20	134	186	2.8	4.2	1	IEEE802.3at
MLP 3x3	FDMC86248	150	20	90	125	3.4	6.4	1.7	IEEE802.3at
MLP 3X3	FDMC86240	150	20	51	70	4.6	11	2.3	IEEE802.3at
MLP 3X3	FDMC86260	150	20	34	44	5.4	15	3.1	IEEE802.3at
MLP 5X6	FDMS86252	150	20	51	70	4.6	11	2.4	IEEE802.3at
MLP 5X6	FDMS86250	150	20	25	33	6.7	25	5.5	IEEE802.3at
MLP 5X6	FDMS86200	150	20	18	21	9.6	33	7.7	IEEE802.3at
DPAK	FDMS86252	150	20	52	72	5	11.3	2.6	IEEE802.3at

Power over Ethernet – MOSFETs for PD

Q5 Synchronous Rectification MOSFETs

Package	Part Number	BVdss (V)	V_{GS} (V)	$R_{DS(ON)}$ Max (mΩ) @10Vgs	$R_{DS(ON)}$ Max (mΩ) @6Vgs	I_D (A)	Q_G (nC) @10Vgs	Q_{GD} (nC)	Remark
SSOT3	FDN537N	30	20	23	30	6.5	5.3	0.8	IEEE802.3af
SSOT6	FDC366BN	30	20	25	33	6.3	9	1.6	IEEE802.3af
MLP 3X3	FDMC7692S	30	20	9.3	13.6	12.5	16	2	IEEE802.3at SyncFET
MLP 3X3	FDMC8651	30	20	6.1	9.3	15	19.4	4.2	IEEE802.3at
MLP 3X3	FDMC8023S	30	20	4.4	5.2	19	37	6	IEEE802.3at SyncFET
MLP 3X3	FDMC86012	30	20	2.7	4.7	23	27	5.4	IEEE802.3at
MLP 3X3	FDMC8010	30	20	1.3	1.8	30	67	9.5	IEEE802.3at
MLP 5X6	FDMS8026S	30	20	4.3	5.2	19	27	3.7	IEEE802.3at SyncFET
MLP 5X6	FDMS8820	30	20	2	2.4	28	63	8.2	IEEE802.3at
MLP 3X3	FDMC86520L	60	20	7.9	11.7@4.5Vgs	13.5	45	4.9	IEEE802.3at Logic gate
MLP 5X6	FDMS86500L	60	20	2.5	3.6@4.5Vgs	25	117	11.5	IEEE802.3at Logic gate
MLP 3X3	FDMC86324	80	20	23	37	7	13	3.6	IEEE802.3at
MLP 3X3	FDMC86320	80	20	11.7	16	10.7	29	6.9	IEEE802.3at
MLP 5X6	FDMS86322	80	20	7.65	12	13	39	10.8	IEEE802.3at
MLP 5X6	FDMS86300	80	20	3.9	5.5	19	72	14.9	IEEE802.3at

Power over Ethernet – MOSFETs for PD

Q6 Synchronous Buck Dual MOSFETs

Package	Part Number	BVdss (V)	V_{GS} (V)	$R_{DS(ON)}$ Max (mΩ) @10Vgs	$R_{DS(ON)}$ Max (mΩ) @4.5Vgs	I_D (A)	Q_G (nC) @10Vgs	Q_{GD} (nC)	Remark
MLP 5X6	FDMS3626S	25	12	5	5.7	17.5	26	2.7	Asymmetric dual N
				2.6	3.2	25	41	4.3	
MLP 5X6	FDMS3620S	25	12	4.7	5.5	17.5	26	2.7	Asymmetric dual N
				1	1.2	38	106	12	
MLP 3X3	FDMC8200S	30	20	20	32	6	7.3	1	Asymmetric dual N
				10	13.5	8.5	15.7	1.9	
MLP 5X6	FDMS3668S	30	20	8	11	13	21	2.6	Asymmetric dual N
				5	5.2	18	27	2.5	
MLP 5X6	FDMS3664S	30	20	8	11	13	21	2.6	Asymmetric dual N
				2.6	3.2	25	37	4	
MLP 5X6	FDMS3660S	30	20	8	11	13	21	2.6	Asymmetric dual N
				1.8	2.2	30	62	7	

Power over Ethernet – Resources

Application Notes and Demo Boards

Application Notes	
AN-4154	MOSFETs for 60W High-Power PoE applications http://www.fairchildsemi.com/an/AN/AN-4154.pdf
AN-9759	GreenBridge™ MOSFETs to Replace Conventional Diode Bridge in Power over Ethernet Applications http://www.fairchildsemi.com/an/AN/AN-9759.pdf
Demo Boards	
AN-FEBFDMQ8203-13W	User Guide for FEBFDMQ8203_13 W GreenBridge™ MOSFETs Evaluation Kit for Power Over Ethernet 13 W Flyback DC-DC http://www.fairchildsemi.com/an/AN/AN-FEBFDMQ8203-13W.pdf
AN-FEBFDMQ8203-25W	User Guide for FEBFDMQ8203_25 W GreenBridge™ MOSFETs Evaluation Kit for Power Over Ethernet 25 W Flyback DC-DC http://www.fairchildsemi.com/an/AN/AN-FEBFDMQ8203-25W.pdf
AN-FEBFDMQ8203-30W	User Guide for GreenBridge™ MOSFETs Evaluation Kit for Power over Ethernet 30W Active Clamp Forward DC-DC http://www.fairchildsemi.com/an/AN/AN-FEBFDMQ8203-30W.pdf

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